CLAIMS

What is claimed is:

1. In a data processing system including a cache memory and a system memory coupled to a processor, a method for executing a computer program, comprising, in response to executing an instruction that references data in the system memory and that specifies an alternate control path:

determining whether the data referenced in the instruction are present in the cache memory; and

changing control flow of the program in accordance with the specified alternate control path if the referenced data are not present in the cache memory.

2. The method of claim 1, further comprising:

returning the data referenced in the instruction from the cache memory to the processor if the referenced data are present in the cache memory; and

returning the data referenced in the instruction from the system memory to the processor if the referenced data are not present in the cache memory.

3. The method of claim 2, wherein changing control flow further comprises branching to a program address specified by the instruction.

4. The method of claim 2, wherein changing control flow further comprises skipping an instruction.

5. The method of claim 1, further comprising returning the data referenced in the instruction from the cache memory to the processor only if the referenced data are present in the cache memory.

6. The method of claim 5, further comprising, if the referenced data are not present in the cache memory, loading the data referenced in the instruction from the system memory to the cache memory.

7. The method of claim 5, further comprising if the referenced data are not present in the cache memory, bypassing loading of the data referenced in the instruction from the system memory to the cache memory.

8. The method of claim 5, wherein changing control flow further comprises branching to a program address specified by the instruction.

9. The method of claim 5, wherein changing control flow further comprises skipping an instruction.

10. The method of claim 1, further comprising:

if the data are present in the cache memory, bypassing loading of the referenced data from the cache memory to the processor;

if the data are not present in the cache memory, bypassing loading of the referenced data from the system memory to the cache memory.

11. The method of claim 10, wherein changing control flow further comprises branching to a program address specified by the instruction.

12. The method of claim 10, wherein changing control flow further comprises skipping an instruction.

13. The method of claim 1, wherein changing control flow further comprises branching to a program address specified by the instruction.

14. The method of claim 1, wherein changing control flow further comprises skipping an instruction.

15. A computing arrangement comprising:

a processor configured to execute a program;

a cache memory coupled to the processor;

a system memory coupled to the cache memory, wherein the processor is configured to execute an instruction that references data in the system memory and that specifies an alternate control path in the program;

means for determining whether the data referenced in the instruction are present in the cache memory; and

means for changing control flow of the program in accordance with the specified alternate control path if the referenced data are not present in the cache memory.